PATENT APPLICATION

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

ATTORNEY DOCKET NO. ___10015698 -4___

Inventor(s):   Blaine D. Gaither

Application No.: 10/649917

Filing Date: Aug 26, 2003

Confirmation No.: 6774

Examiner: Dinh, Ngoc V.

Group Art Unit: 2189

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NOV 1 4 2005

Title: Cache System With Groups Of Lines And With Coherency For Both Single Lines And Groups Of Lines

Mail Stop Amendment
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Transmitted herewith is/are the following in the above-identified application:

[X] Response/Amendment
[X] New fee as calculated below
[ ] No additional fee
[X] Other Terminal Disclaimer

[ ] Petition to extend time to respond
[ ] Supplemental Declaration

Fee$ 130

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	9	MINUS	20	= 0	X $50	$ 0
INDEP. CLAIMS	6	MINUS	7	= 0	X $200	$ 0
[ ] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM				+ $360		$ 0
EXTENSION FEE	[ ] 1st Month $120	[ ] 2nd Month $450	[ ] 3rdMonth $1020	[ ] 4th Month $1590		$ 0
					OTHER FEES	$ 130
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 130

Charge $___130___ to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (571) 273-8300.
Date of facsimile: November 14 2005

Typed Name: Donna M Kraft
Signature: Donna M Kraft

Respectfully submitted,

Blaine D. Gaither

By A. W. Winfield

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Rev 10/05 (TransAmdFax)

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NOV 1 4 2005

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):   Blaine D. Gaither

Serial No.:   10/649,917

Filing Date: 08/26/2003

Title: CACHE SYSTEM WITH GROUPS OF LINES AND WITH COHERENCY FOR BOTH
SINGLE LINES AND GROUPS OF LINES

Examiner: Dinh, Ngoc V.

Group Art Unit: 2189

AMENDMENT

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

Amendments to the claims are reflected in the listing of claims beginning on page 2.

Remarks begin on page 4 of this paper.

— 1 —

1. (original) A computer system, comprising:

a cache memory that reads and caches a group of lines with a single memory transaction; and

a system for maintaining identity of which device, if any, owns the group of lines, and which device, if any, owns each individual line within the group of lines.

2. (original) The computer system of claim 1, the system for maintaining identity of which bus, if any, owns each individual line within the group of lines.

3. (original) The computer system of claim 1, further comprising:

at least two lines in the group of lines having separate owners.

4. (original) A computer system, comprising:

a cache memory that reads a group of lines with a single memory transaction; and

the cache memory receiving fewer than all lines within the group of lines, when the group of lines is requested, and when the group of lines is partially owned by another cache memory.

5- 6 (canceled)

7. (original) A method of maintaining coherency for a computer system, comprising:

retrieving a group of lines in response to a request for a single line; and

maintaining ownership information for the group of lines and for each individual line within the group of lines.

8. (original) A method of transferring lines of memory in a computer system, comprising:

requesting, by a processor, a line of memory;

copying, from a shared memory, to a cache memory, the line of memory requested;

copying, from the shared memory to the cache memory, all additional unowned lines within a group of lines corresponding to the requested line, and not copying any owned lines, other than the requested line, within the group of lines.

9. (original) The method of claim 8, further comprising:

setting a coherency state, within the cache memory, of an entry location for a line in the group of lines that is not copied, to a state that indicates that the contents of the entry location are invalid.

10. (original) A method for maintaining coherency for a computer system, comprising:

(a) requesting, by a processor, a line of memory, the line of memory within a group of lines;

(b) detecting that all lines in the group of lines have been modified by one owner;

(c) copying, in response to the request of step (a), all the lines in the group of lines to a cache memory for the processor; and

(d) setting a coherency state, within the cache memory, of all lines in the group of lines, to a state that indicates that the lines are owned by the cache memory.

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